ABSTRACT

A self-timed data communication system for a wide data width semiconductor memory system having a plurality of data paths is provided. The data communication system includes a central data path including at least one junction circuit configured for exchanging data signals between the central data path and the plurality of data paths of the at least one data path. A respective one junction circuit of the at least one junction circuit includes circuitry for controlling resetting the respective one junction circuit for preparation of a subsequent data transfer through the respective one junction circuit in accordance with receipt of an input junction monitor signal indicating that data has been transferred to the respective one junction circuit. The data communication system further includes a plurality of data banks configured for storing data, wherein a corresponding data bank of the plurality of data banks is connected to a respective one data path of the plurality of data paths. The data communication system further includes circuitry for controlling the respective one data path in accordance with receipt of a monitor signal indicating that a data transfer operation has been initiated for transfer of data from the respective one data path. The circuitry for controlling includes circuitry for generating a control signal for controlling resetting of the respective one data path after data is transferred for preparation of a subsequent data transfer operation.